INTEL® SPECIFICATION ADDENDUM FOR THE JEDEC DDR200 REGISTERED DIMM SPECIFICATION

Rev. 1.0

June 11, 2001

Table of Contents

Revision History

Rev.	Description	Date
0.9	Initial Release	Feb 2, 2001
1.0	Final Release	June 11, 2001

Objective

This Specification addendum calls out changes to the JEDEC DDR SDRAM Registered DIMM Design Specification Rev 1.0 (dated July 2000, JEDEC ballot JC-42.5-00-113). The intent of this document is to clarify and detail specifications for DDR Memory.

This addendum applies specifically to raw cards A, B and C. No review has been done for those parts of the JEDEC specification referring to raw cards E, F, H and K. The DDR component must meet the JEDEC DDR SDRAM specification Rev 0.9 (dated 7/20/99), as modified by the Intel DDR 200 JEDEC Specification Addendum.

Note: Page number references are to the JEDEC DDR SDRAM Registered DIMM Design Specification Rev 1.0.

Product Description (pg. 1)

This specification defines the electrical and mechanical requirements for the 184-pin, 2.5 Volt, DDR 200/DDR 266, 72-bit wide, Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR SDRAM DIMMs).

Product Family Attributes

DIMM dimensions	5.25" x 1.7" x .157"/.268"/.320"[1]
SDRAMs supported	64Mb, 128Mb, 256Mb, 512Mb, 1Gb
Serial Presence Detect EEPROM	Ballot JCB-00-02

Note 1. 0.157" for TSOP, 0.268" for stacked TSOP, 0.320" for stacked TSOJ

Architecture (pg. 2)

Pin Description

The following have been added to the pin description table:

Pin Name	Description
A0-A13	SDRAM address bus
DU	Do Not Use (may be connected to an active signal on the baseboard)
SCL	I^2C serial bus clock for EEPROM
SDA	I^2C serial bus data line for EEPROM
SA0-SA2	I^2C slave address select for EEPROM

Input/Output Functional Description (pg. 3)

Symbol	**Type**	**Function**
SA0-2		Tied to V_{SS} or V_{DDSPD}
SDA	Open collector	A pullup resistor on the baseboard must be connected from the SDA bus line to V_{DDSPD}.
SCL	Open collector	A pullup resistor on the baseboard may be connected from the SCL bus line to V_{DDSPD} or, SCL may be driven by a single I^2C master.
V_{DDSPD}	Supply	Serial EEPROM positive power supply (wired to a separate pin at the connector, which supports operation from a minimum of 2.3V to a maximum of 3.6V)

184-Pin DDR SDRAM DIMM Pin Assignments (page 4)

Pin #	X64 Non-Parity	X72 ECC
103	NC(FETEN)	NC(FETEN)
167	A13	A13

Differential Clock Net Wiring (CK0, /CK0) (pg. 15)

Raw Card	Organization	First 8 clock pairs	Ninth clock pair
Card A (single bank)	x64	One DRAM, one padding capacitor[1]	Two padding capacitors[1]
	x72	One DRAM, one padding capacitor[1]	One DRAM, one padding capacitor[1]
Card A (double bank) Card B	x64	Two DRAMs	Two padding capacitors[1]
	x72	Two DRAMs	Two DRAMs
Card C	x72	Four DRAMs	Four DRAMs

Note 1: Padding capacitor is 1.25 pF ± 20% to 2 pF ± 20%.

Register Functional Assignments (pg. 16)

Raw Card Versions A, B (Two 1:1 Registers)				Raw Card Version C (Two 1:2 Registers)			
Register 1		Register 2		Register 1		Register 2	
In	Out	In	Out	In	Out	In	Out
A1	RA1	A0	RA0	:	:	A13[2]	RA13A[2]
:	:	A10	RA10				RA13B[2]
:	:	A13[2]	RA13[2]			:	:

On the current raw cards A and B, address A1 was moved from Register 2 to Register 1, due to routing congestion in between the “key” and the PLL clock buffer.

Note 2: Only used with 1Gb SDRAMs.

Component Details (pg. 17 and 18)

Pin Assignments for 64Mb, 128Mb, 512Mb and 1Gb DDR SDRAM Planar Components

For pin 17, replace NC with A13.

Pin Assignments for 64Mb, 128Mb, 512Mb and 1Gb DDR SDRAM 2 High Stack Package

For pin 17, replace NC with A13.

DIMM PLL Use (pg. 20)

Raw Card Version	# of Banks	# of SDRAMs per output	PLL Type	Quantity
A	1	$2^{1,2}$	1:10, 2.5Volt	1
	2	2^{2}	1:10, 2.5 Volt	1

Note 2: In the case of the x64 card, padding capacitors are used in the unpopulated DRAM locations.

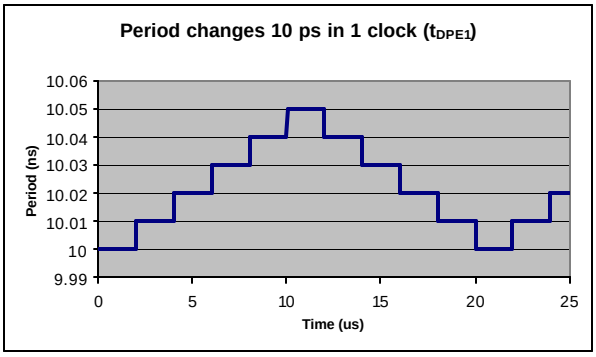
Critical CDC857 PLL Specifications (pg. 21)

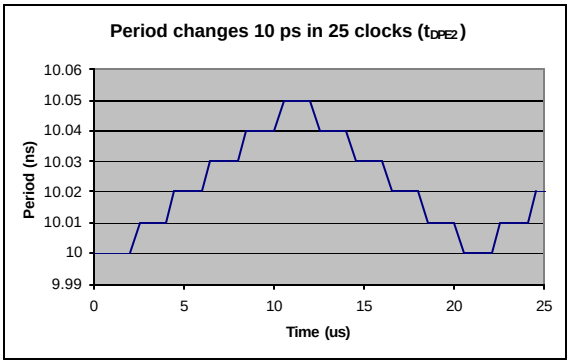
Device	Symbol	Parameter	Conditions	T_A = 0-70° C V_{DD} = 2.5V ± 0.2V		Units	Notes
				Min	Max		
1:10, 2.5V	f_{CK}	Operating Clock Frequency		60	170	MHz	1
	f_{CK}	Application Clock Frequency		95	170	MHz	1
	t_{SPE}	Static Phase Error		-120	120	ps	2
	t_{DPE1}	Dynamic Phase Error	10 ps step in period	-200	200	ps	2,5
	t_{DPE2}	Dynamic Phase Error	10 ps ramp in period over 250 ns	-30	30	ps	2,5

Note 1: The PLL used on the registered DIMM needs to support SSC synthesizers with a Modulation Frequency of 30 to 50 KHz and a Clock Frequency Deviation of –0.5% (period deviation of +0.5%.). PLL designs should target the following values:

- Greater than **2 MHz** PLL loop bandwidth
- Less than –0.031 degrees of phase angle

Note 5: The Dynamic Phase Error is the spread spectrum clocking induced skew between the input clock pair and the feedback clock pair, excluding static phase error, input clock jitter and output clock jitter. It is a function of the step size of the spread spectrum input clock period, and how many clocks that step takes place over. The following diagrams illustrate the input clock (with jitter removed) going from its nominal 10 ns to its maximum of (10 ns + 50 ps) in five 10 ps steps, and then returning to the nominal value in another five 10 ps steps. For t_{DPE1}, the input clock changes its period in a single clock, while for t_{DPE2}, the input clock changes its period over 250 ns (25 clocks at 100 MHz.)





PLL Sourcing (pg. 21)

The functionality and the technical requirements of this part have been standardized by JEDEC and the relevant standard is JESD82, dated July 2000.

Resistor tolerances (pg. 32, 36 and 37)

DQ/DQS/DM Series Resistor		
Type	**Card**	**Series Resistor**
DDR 200	A,B	22 ± 5%
	C	22 ± 2%

Net Structure Routing for PLL Output to SDRAM Load (pg. 34)

Note: Refer to differential clock wiring on page 15 for use of padding caps whenever an SDRAM is not stuffed in a location.

DIMM Post-Register Timing (pg. 51)

Symbol	Parameter	Time (ns) Set-up	Time(ns) Hold	Notes
t_{PD}	Maximum (minimum) time ….	-2.8	1.1	
$t_{NETDELAY}$	Maximum (minimum) time ….	-2.0	0.5	
t_{REG}	Shift in the register clock in relationship to the SDRAM…	-0.10	-0.10	
Margin		**3.275**	**0.2**	**1**

Serial Presence Detect Example Raw Card Version 'A' (pg. 52, 53)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
22	SDRAM Module Attributes: General	V_{DD} ± 0.2, t_{RAS} lockout, Concurrent Auto-precharge	C0	Bit 7 = 1 for t_{RAS} lockout enabled, Bit 6 = 1 for concurrent auto-precharge enabled
36-40	Reserved	Undefined	00	
41	t_{RC}	70.0ns	46	
42	t_{RFC}	80.0ns	50	
43	t_{Ckmax}	12.0ns	30	
44	t_{DQSQ}	600 ps	3C	
45	t_{QHS}	1000 ps	A0	
46-59	Reserved	Undefined	00	
60-61	Reserved	Undefined	00	

DIMM Mechanical Specification (pg. 55)

PLL Pin 1 dot needs to be in the lower left.

Power Decoupling Design Guidelines (new)

This table reflects the decoupling indicated in the “Bill of Materials” accompanying the databases for raw cards A1, B2 and C2.

Supply	Quantity	Value	Tolerance	Type
V_{DD}	9	2.2 nF	± 20%	X7R
	52-61	220 nF	± 20%	X7R
	4	2.2 uF	+80%/-20%	Y5V
V_{REF}	12	220 nF	± 20%	X7R

Serial Presence Detect Component Specification (new)

The DIMM vendor should ensure that the lower 128 bytes can be software write protected. A write to the SPD with address "0 1 1 0 SA2 SA1 SA0 0", where SA(2:0) are the SPD addresses on the DIMM connector, will prevent all future writes to the lower 128 bytes of the SPD. The software write protect feature is "write once", but should be done by the BIOS at each power up, to prevent corruption of the lower 128 bytes of the SPD.